Evaluation Board for the ADV7172/73 Digital Video Encoder

Eval-ADV7172/73EB V3.1 10/98

FEATURES On-Board Reference On-Board Clock 8bit CCIR656/601 Pixel Data Input 6 analog video outputs Direct Hook-Up to Printer Port of PC PC Software for Control of the ADV7172/73 modes

INTRODUCTION

This Application Note describes the ADV7172/73EB evaluation board which supports the ADV7172/73 Digital Video Encoder. The device accepts CCIR601/656 compatible video data and converts into analog Composite, Y/C, RGB or YUV video signals in PAL

REQUIREMENTS

The ADV7172/73 evaluation board requires a DC power supply which is able to deliver a minimum of 5V. Current requirements are approx. 0.3 A. To run the software which is supplied with the ADV7172/73 it is necessary to connect the printer port LPT1 of the PC to the boards 36pin

GENERAL DESCRIPTION

The ADV7172/73EB provides a 25-pin input port, J1, over which pixel data in CCIR601/656 format can be input. Test pattern generators providing these standards are the Tektronix TSG601 handheld signal generator or the Tektronix TPG20. The input pixel data is converted from ECL level to TTL level via the MC10125TTLs (U1, U2, U3).

If a different clock source as that provided by the pixel data is required, the ADV7172/73EB features a 27Mhz clock (X1) which can be connected over jumper LK5.

The on-board push-button, SW1provides control over the $\overline{\text{RESET}}$ pin. When this button is pressed, the internal registers of the ADV7172/73 reset to default register settings (see following page).

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Centronics connector, J10. In order to run the software on a PC the operating system needs to be Windows 95 or Windows 98. The system requirements ask for any Pentium I, PMMx or Pentium II PC.

The ADV7172/73EB also features an external Voltage Reference (D1) which provides 1.235V Output Voltage.

The outputs of DAC D, E, F are fed to an AD817 buffer op-amp (U6-8) followed by a passive low-pass filter before being output over the BNC connectors. The outputs of DAC A, B, C are directly fed to a LPF and then output over the BNC connectors.

The ADV7172/73 pins can be accessed independently over header JP1.

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REGISTER SETTINGS ON POWER-UP AND ON RESET

After pressing the reset button SW1on the evaluation board, the register settings of the ADV7172/73 will set up as follows:

NTSC Video Standard. DAC A, B, C off DAC D, E, F on

Disabled:

- MR1: Low Power mode
- MR2: Sleep Mode Control, Pixel Data Valid, Standard I2C, Square Pixel, SCART
- MR3: Closed Captioning, TTX Bit Request, Teletext, VBIOpen
- MR4: Color Bars, VSYNC_3H
- MR5: CLAMP, RGB Sync, Y-Level Control
- MR7: Sharpness Control, Brightness Control, Hue Adjust, Luma Saturation, Color Control

Enabled:

MR2: Pedestal

MR3: Active video filter

MR4: Burst, Chrominance

MR6: Power-Up Sleep Mode

Output Configuration:

DAC A: G DAC B: B DAC C: R DAC C: R DAC D: CVBS DAC E: LUMA DAC F: CHROMA

Timing Mode 0, Slave, Blank Input Enabled, Interlaced Mode, normal operating mode (no genlock), UV default levels, TTX input, HSO Out.

Subcarrier	Frequency	Register	0:	16hex
Subcarrier	Frequency	Register	1:	7Chex
Subcarrier	Frequency	Register	2:	F0hex
Subcarrier	Frequency	Register	3:	21hex

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The following register settings will correspond to the above settings:

00hex	MR0	00hex
01hex	MR1	07hex
02hex	MR2	08hex
03hex	MR3	00hex
04hex	MR4	00hex
05hex	MR5	00hex
06hex	MR6	00hex
07hex	MR7	00hex
0Chex	SFR0	16hex
0Dhex	SFR1	7Chex
0Ehex	SFR2	F0hex
0Fhex	SFR3	21hex

all other registers : 00hex

After powering up the ADV7172/73EB a hardware reset should be applied (SW1).

EVALUATION SOFTWARE

In order to give the user complete control over the ADV7172/73, a computer program is supplied with the board.

Setting Up:

Insert DISK 1 into the floppy drive and double click on "SETUP.EXE" and you will be prompted for all other necessary information.

Running the Software:

Double clicking the ADV7172/73 icon will run the software for the evaluation board.

Initialisation:

To output NTSC colorbars on DAC A after power up the following settings should be implemented:

Enable DAC A Enable Pixel Data Valid Enable Standard I2C Large DACs set to Comp / Y/C Enable Colorbars

Jumper LK5 set to XTAL Jumper LK4 set to LO Jumper LK8 inserted Jumper LK7 set to RESET1 No jumper on LK1, LK2, LK3, LK9

Otherwise it is recommended to consult the datasheet for information about each control.

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IMPORTANT THINGS TO KNOW:

Validity of Settings:

The evaluation software can automatically check for an acknowledge or, when any register is changed can automatically read-back the new value stored in that register. The "ACKcheck" function is in the "Options" menu. The "Continuous Read" function may be enabled in the "Register Access" menu.

I²C Compatible Programming:

This version of software does not take into account the ability of the ADV7172/73 to accept continuous streams of data. Instead, for every register write or read, it completely re-initiates a start sequence (see the ADV7172/73 Data sheet for information on different ways registers can be written to). This means that more information has to be written to the MPU port extending the time required to program the ADV7172/73.This, while being a valid way of writing to the ADV7172/73 is not the optimum method of writing to the ADV7172/73.

Dynamically Linked Menu System:

All menues in this software are interactive, so when (for example) you change the value of a register all switch settings relevant to that register change will automatically change to the correct state, the inverse is also correct.

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ADV7172/73 LINKS

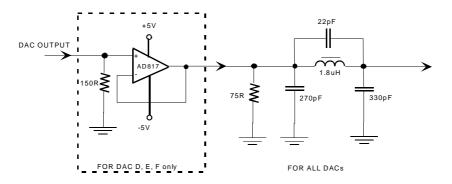
These links are used for operating the ADV7172/73 encoder:

- LK1 Connect BLANK pin to ground.
- LK2 Connect VSYNC/FIELD to ground.
- LK3 Connect HSYNC to ground.
- LK4 Tie ALSB pin high (HI) or low (LO).
- LK5 Connect to XTAL for internal colorbars.

Connect to EXT for pixel input.

- LK7 Connect to LK7 for Rset1 = 150 Ohms Connect to RSet1 for Rset1 = 600Ohms
- LK8 Connect PAL_NTSC pin to ground.
- LK9 Connect SCRESET/RTC to ground.

External Filter and Output Buffer



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